Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A power amplifier integrated circuit consisting essentially of:

a plurality of transistors each comprising a base;

a plurality of ballast resistors corresponding to the plurality of transistors, each ballast resistor having a first terminal and a second terminal, the first terminal connected to the base of the corresponding transistor;

a DC node to which the second terminals of the plurality of ballast resistors are connected;

an RF node for supplying an RF input signal; and

a capacitor having a third terminal and a fourth terminal, the third terminal connected to the RF node and the fourth terminal connected to the plurality of bases.

[c2] 2. The power amplifier integrated circuit of claim 1 wherein the transistors are heterojunction bipolar transistors.

[c3] 3. The power amplifier integrated circuit of claim 1 wherein the capacitor has a substantially high capacitance so that the RF input signal applied at the RF node suffers low signal loss through the power amplifier inte-

grated circuit.

[c4] 4. The power amplifier integrated circuit of claim 1 wherein the capacitor comprises two regions of metallization in two different layers of a semiconductor.

[c5] 5. The power amplifier integrated circuit of claim 1 wherein the ballast resistors are set to maximize uniformity of temperature of a plurality of emitters of the transistors.

[c6] 6. The power amplifier integrated circuit of claim 1 being a portion of a wired or wireless system application.

[c7] 7. The power amplifier integrated circuit of claim 1 being a portion of a mobile telephone.

[c8] 8. A semiconductor devicecomprising:
a semiconductor substrate;
a DC node for receiving a DC voltage;
an RF node for receiving an RF input signal;
a plurality of transistors formed on the semiconductor substrate, each of the plurality of transistors having a base;
a plurality of ballast resistors formed on the semiconductor substrate and corresponding to the plurality of transistors, each ballast resistor having a first terminal and a second terminal, the first terminal connected to

the base of the corresponding transistor, the second terminal connected to the DC node; and
a capacitor formed on the semiconductor substrate, the capacitor having a third terminal and a fourth terminal, the third terminal connected to the RF node and the fourth terminal connected to more than one of the plurality of bases.

[c9] 9. The semiconductor device of claim 8 wherein the transistorsare heterojunction bipolar transistors.

[c10] 10. The semiconductor device of claim 8 wherein the capacitor comprises two regions of metallization in two different layers of the semiconductor device.

[c11] 11. The semiconductor device of claim 8 wherein the capacitor comprises a first region of metallization in a first layer and a second region of metallization in a second layer different from the first layer, the first terminal of the ballast resistor is connected to the base of the corresponding transistor in the first region, and the fourth terminal of the capacitor is connected to more than one of the plurality of bases in the second region.

[c12] 12. The semiconductor device of claim 8 further comprising additional pluralities of transistors and ballast resistors and corresponding capacitors, wherein sets of

an equal number of the transistors and ballast resistors and a capacitor form a power amplifier integrated circuit.

[c13] 13. The semiconductor device of claim 12 wherein each set comprises four transistors, four ballast resistors, and one capacitor.